CLAIMS

Having thus described our invention, what we claim as new and desire to secure by Letters Patent is:

1. A method for producing a test device for silicon-on-insulator (SOI) material comprising:

a) providing a protective mask layer in the shape of an array of isolated mesas over a Si surface of the SOI material;

b) removing Si material not protected by the protective mask layer to form an array of isolated Si mesas in the Si surface;

c) removing the protective mask layer from the array of isolated Si mesas in the Si surface; and

d) forming a pair of electrodes within each Si mesa of the array of isolated Si mesas by depositing one or more metal layers on each Si mesa.

2. The method of claim 1, including forming the array of isolated Si mesas on a top Si surface of the SOI material, and depositing a metal layer on a bottom Si surface of the SOI material.

3. The method of claim 1, wherein the step of depositing deposits one or more metal layers from the group consisting of Al, Er, Gd, Nd, Ti, Y, Ag, Au, Cr, Cu, Ni and Pt.

4. The method of claim 1, further including the step of irradiating a Si surface of the test device with light having a wavelength shorter than the bandgap wavelength of the Si surface.

5. A method for producing a test device for silicon-on-insulator (SOI) material comprising:

a) providing a gate insulator on a Si surface of the SOI material;

b) forming an electrode structure by depositing a first metal electrode layer from the group consisting of Al, Er, Gd, Nd, Ti and Y, followed by depositing a second metal layer from the group consisting of Ag, Al, Au, Cr, Cu, Mg, Ni and Pt;

c) annealing the electrode structure at an elevated temperature in an inert atmosphere;

d) depositing a gate electrode layer on the gate insulator;

e) providing a protective mask layer over the electrodes in the shape of an array of isolated mesas;

f) removing Si material not protected by the protective mask layer to form an array of isolated Si mesas in the Si surface; and

g) removing the protective mask layer from the array of isolated Si mesas in the Si surface.

6. The method of claim 5, wherein the annealing step is carried out at a temperature of 440 to 475°C for a period of 5 to 15 minutes in an inert atmosphere.

7. The method of claim 5, wherein the step of providing a protective mask layer includes providing a protective layer of photoresist over the electrodes and Si surface.

8. The method of claim 7, further including using a mask to form the layer of photoresist into a protective mask layer having the shape of an array of isolated mesas on the Si surface.

9. The method of claim 5, further including the step of irradiating a Si surface of the test device with light having a wavelength shorter than the bandgap wavelength of the Si surface.

10. A method for fabricating double gate FET test structures for electrical evaluation of a semiconductor layer on a buried oxide on a Si substrate comprising:

a) providing a gate insulator on a surface of the semiconductor layer;

b) depositing source and drain metal electrodes on the gate insulator in a geometric pattern, including depositing a first metal electrode layer from the group consisting of Al, Er, Gd, Nd, Ti, and Y, followed by depositing a second metal layer from the group consisting of Ag, Al, Au, Cr, Cu, Mg, Ni, and Pt, to form an electrode structure;

c) annealing the electrode structure at an elevated temperature in an inert atmosphere;

d) depositing a gate electrode between the source and drain metal electrodes without contacting the source and drain metal electrodes;

e) depositing a protective layer over the entire Si surface;

f) creating individual isolated mesas of the protective layer to form a protective mask layer on the Si surface with the source, drain, and gate electrodes residing within the boundaries of the mesas;

g) removing the gate insulator and the semiconductor layers in regions between the mesas;

h) removing the protective mask layer.

11. The method of claim 10, wherein the annealing step is carried out at a temperature of 440 to 475°C for a period of 5 to 15 minutes in an inert atmosphere of N2 and H2.

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12. The method of claim 10, including depositing a protective layer of photoresist.

13. The method of claim 10, including covering the protective layer of photoresist with a metal layer evaporated through a mask to form a protective mask to cover and mask the individual isolated mesas.

14. The method of claim 10, including fabricating the test structures as an array of individual test mesa structures.

15. The method of claim 10, including depositing the gate electrode as a metal film less than 30 nm thick.

16. The method of claim 10, wherein the semiconductor layer contains a region of strained Si.

17. The method of claim 10, wherein the semiconductor layer contains regions of strained Si and SiGe.

18. The method of claim 10, wherein the semiconductor layer contains a region of one or more layers made from compounds from the III and V columns of the periodic table.

19. The method of claim 10, further including the step of irradiating a Si surface of the test device with light having a wavelength shorter than the bandgap wavelength of the Si surface.

20. A method for fabricating double gate FET test structures for electrical evaluation of a strained Si layer on a SiGe layer on a buried oxide on a Si substrate comprising:

a) providing a gate insulator on a surface of the strained Si layer;

b) depositing source and drain metal electrodes in a geometric pattern, including depositing a first metal electrode layer from the group consisting of Al, Er, Gd, Nd, Ti

and Y, followed by depositing a second metal layer from the group consisting of Ag, Al, Au, Cr, Cu, Mg, Ni and Pt to form an electrode structure;

c) annealing the electrode structure at an elevated temperature in an inert atmosphere;

d) depositing a gate electrode on the gate insulator between the source and drain metal electrodes without contacting the source and drain metal electrodes;

e) depositing a protective layer over the entire Si surface;

f) creating individual isolated mesas of the protective layer to form a protective mask layer on the Si surface with the source, drain, and gate electrodes residing within the boundaries of the mesas;

g) removing the gate insulator, the strained Si and the SiGe layers from regions between the mesas;

h) removing the protective mask layer.

21. The method of claim 20, wherein the annealing step is carried out at a temperature of 440 to 475°C for a period of 5 to 15 minutes in an inert atmosphere of N2 and H2.

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22. The method of claim 20, including depositing a protective layer of photoresist.

23. The method of claim 22, further including covering the protective layer of photoresist with a metal layer evaporated through a mask to form a protective mask to cover and mask the individual isolated mesas.

24. The method of claim 20, including fabricating the test structures as an array of individual test mesa structures.

25. The method of claim 20, including depositing the gate electrode as a metal film less than 30 nm thick.

26. The method of claim 20, including depositing the gate electrode as a transparent conductive material.

27. The method of claim 20, further including the step of irradiating a Si surface of the test device with light having a wavelength shorter than the bandgap wavelength of the Si surface.

28. A process for creating offset multiple layers of source and drain metal electrodes in an FET device test structure comprising:

a) positioning a patterned shadow mask separated from the surface of the test structure by a distance of at least 0.5 millimeters;

b) depositing a first metal electrode of a metal having a low barrier height for electrons from a first metal source through the patterned shadow mask onto the test structure; and

c) depositing a second metal electrode of a metal having a low barrier height for holes from a second metal source through the patterned shadow mask onto the test structure.

29. The process of claim 28, including depositing the first metal electrode from a group consisting of Al, Er, Gd, Nd, Ti and Y which has a low barrier height for electrons, and depositing the second metal electrode from a group consisting of Ag, Al, Au, Cr, Cu, Mg, Ni and Pt which has a low barrier height for holes.

30. The process of claim 28, for creating offset multiple layers of source and drain metal electrodes in a single gate ring FET device test structure.

31. The process of claim 28, for creating offset multiple layers of source and drain metal electrodes in a double gate ring FET device test structure.

32. An FET device comprising a source electrode and a drain electrode, wherein each of the source electrode and the drain electrode comprises first and second metals which are formed contacting each other while being offset relative to each other, the first metal comprises an ohmic metal which has a low barrier height for electrons, and the second metal comprises an ohmic metal which has a low barrier height for holes, such that both electron and hole electrical properties can be measured from the offset metal electrodes.

33. The FET device of claim 32, wherein the first metal comprises an ohmic metal from the group consisting of Al, Er, Gd, Nd, Ti and Y which has a low barrier height for electrons, and the second metal comprises an ohmic metal from the group consisting of Ag, Al, Au, Cr, Cu, Mg, Ni and Pt which has a low barrier height for holes.

34. The FET device of claim 32, in a double gate FET.

35. The FET device of claim 32, in a single gate FET.